IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/689,348	Confirmation No. 4206
Applicant:	:	Stephan Grunow, et al.	
Filed:	:	October 20, 2003	
Art Unit:	:	2891	
Examiner:	:	Dana Farahani	
Docket No.	:	TI-36564	
Customer No.	:	23494	

APPEAL BRIEF UNDER 37 C.F.R. 1.192

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final rejection mailed January 25, 2006, and the Advisory Action mailed March 22, 2006.

Real Party in Interest under 37 C.F.R. 41.37(c)(1)(i)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 41.37 (c)(1)(ii)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 41.37 (c)(1)(iii)

Claims 1, 2, 3 and 15 – 16 are being appealed. Claim 4 was canceled. Claims 1, 2, 3 and 15-16 are rejected.

Status of Amendments Filed After Final rejection under 37 C.F.R. 41.37 (c)(1)(iv)

Appellants filed a response under 37 C.F.R. 1.116 on October 23, 2003 arguing the patentability of claims 1, 2, 3 and 15-16 over the cited prior art. The Examiner upheld the earlier rejection citing that the request for reconsideration was considered but does NOT place the application in condition for allowance.

Summary of the Invention under 37 C.F.R. 41.37(c)(1)(v)

As shown in Figure 2(a) and described on page 6, starting on line 10, of the invention disclosure, a low K dielectric layer 20 is formed above a semiconductor substrate 10. The low K dielectric has a dielectric constant of approximately $\leq$ 3.7 (page 6, line 20). A contiguous non-conformal barrier layer 70 shown in Figure 2(a) is formed in trenches 80, 85 that are formed in the low K dielectric layer 20. The barrier layer 70 has dimensions X_1 which represents the thickness of the layer 70 above the upper surface 35 of the low K dielectric layer 20 and X_2 which represents the thickness of the barrier layer 70 on the sidewall 83 of the trenches (page 8, lines 11-17 and shown in Figure 2(a)). Also shown in Figure 2(a) is the dimension X_4 which is the width of the dielectric material separating adjacent trenches. On page 10, lines 2-8 the width X_4 is described in an embodiment of the invention as being less than or equal to 160nm.

In the embodiments of the invention described on page 10, starting at line 14, the ratio of X_1 to X_2 is given as greater than 3 to 2. In a further embodiment the ration of X_1 to X_2 is described as greater than 5 to 2. As further described on page 10 lines 19-22, CVD or ALD can be used to form the barrier layer 70 in the above described ratios when the width of the trench X_3 (shown in Figure 2(a)) is less than or equal to 160nm and/or X_4 is less than or equal to 160nm.

Statement of Issues Presented for Review under 37 C.F.R. 41.37 (c)(1)(vi)

1. Are claims 1-3 and 5-16 properly rejected under 35 U.S.C. 103(a) as unpatentable over Applicants Admitted Prior Art (AAPA) in view of U.S. Patent No. 6, 410, 985 to Chan (Chan)?

Argument under 37 C.F.R. 41.37(c)(1)(vii)

1. Claims 1-3 and 5-16 are not properly rejected under 35 U.S.C. 103(a) as unpatentable over Applicants Admitted Prior Art (AAPA) in view of U.S. Patent No. 6, 410, 985 to Chan (Chan) and are allowable.

The Examiner has rejected claims 1-3 and 5-16 under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA) in view of U.S. Patent No. 6, 410, 985 to Chan (Chan). Appellants assert that the claims under appeal are not obvious in view of the combination and are therefore allowable. Appellants will address each of the Examiner's assertions regarding the patentability of the claims on appeal.

(i) The Examiner asserts that the recited range in the claims on appeal is obvious because one skilled in the art would know to determine the ratio as an optimum value. In support of this the Examiner cites *In re Boesch*, 617 F.2d 272 (CCPA 1980).

It is respectfully submitted that the Examiner's reliance on *In re Boesch*, in the present case in misplaced, because not only are there not any ranges recited in the combination as to the thickness rations between X1 and X2, as was the case in Boesch, but the recited ration is not even recognized to be a result-effective variable in the combination. In *In re Antonie*, 559 F.2d 618, 620 (CCPA 1977), the Court found that the Examiner was in error when he found that the teachings of a reference that stated no optimized ratios whatsoever would render a device having those optimized ratios obvious. The Court stated the examiner's ruling was in error because the reference contained no teaching of any ratios and did not recognize the problem addressed by the application. This is the case here.

The present application is concerned with reducing the shorts between adjacent interconnects that can result from metal migrating through low-k materials by making certain that only a certain amount of metal is deposited on the sidewalls of the interconnect structure. It should be noted that while it is important to reduce the metal on the sidewalls of the interconnect structure; it is also equally important that a certain thickness of metal be formed on the upper surface of the low-k dielectric. This necessitates the ratios that are clearly described in the disclosure. This problem and solution are not addressed in the prior art rejection asserted by the Examiner.

The Chan reference is concerned with filling smaller "V" or "U" shaped trenches with highly conductive metals, such as silver or copper, to thereby achieve a greater interconnect density in a given area. (Col. 2, lines 51-67 and col. 3, lines 1-10). There is no discussion that the Appellants have found that discussed the problem and solution addressed by the present invention. At best, Chan teaches only that due to the difficulty of achieving a build-up of metal on the sidewalls of the narrow trench, one should deposit approximately 300 angstroms of metal. (Col. 5, lines 63-67), and as admitted by the Examiner the AAPA does not teach or suggest how to alleviate the problem addressed by the present invention. Further, there is no suggestion whatsoever of the recited ratios in the combination, and they should not be expected to be taught by the combination because it does not even recognize the problems addressed by the instant invention. Thus, given the combinations failure to recognize the problem and solution and provide, even in a general way, thickness ratios that would address that problem, one skilled in the art would not be motivated to optimize the thickness ratios recited in Claims 1, 7, 11, and 15 based on the combined teachings of Chan and the AAPA.

Accordingly, the asserted combination fails to establish a prima facie case of obviousness with respect to independent claims 1, 7, 11 and 15 and their respective dependent claims.

(ii) The Examiner asserts that the specification contains no disclosure of either the critical nature of the claimed invention or any unexpected results arising therefrom.

In arriving at this position the Examiner is ignoring a significant portion of the teaching of the specification. As shown in Figure 2(a) and carefully described in the specification starting on page 10, line 14, the ratio of the thickness X_1 and X_2 are an essential art of the invention. The barrier layer 70 serves the function of blocking copper diffusion into the low-k dielectric layer. It has been recognized by the Appellants that this barrier is also a source of conductive paths 60 into the low-k dielectric. The Appellants determined that one possible mechanism for the formation of these conductive paths 60 is related to the thickness of the barrier 60 and then invented a method that results in a significant reduction in the conductive paths while maintaining the margins required for subsequent CMP removal of the various metal layers (including the barrier). As clearly described in the specification, the ratios are important to the invention and cannot be ignored by the Examiner. The Examiner's assertions are incorrect and ignore over half the teaching in the specification.

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-3 and 5-16 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper,

including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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APPENDIX

Claims on Appeal under 37 C.F.R. 41.37(c)(1)(viii)

Claim 1: An integrated circuit interconnect structure, comprising:

a low K dielectric layer with an upper surface formed over a semiconductor;

a first trench formed in said low K dielectric layer wherein said trench has sidewalls;

a first contiguous barrier layer formed to a thickness X_1 over said upper surface of said low k dielectric layer and formed to a thickness X_2 on said trench sidewalls wherein X_1 is greater than X_2, wherein the ratio X_1 to X_2 is greater than 3 to 2; and

copper formed over said first contiguous barrier.

Claim 2: The integrated circuit interconnect structure of claim 1 further comprising a second trench comprising sidewalls formed in said low K dielectric layer and separated from said first trench by a distance less than 160nm.

Claim 3: The integrated circuit interconnect structure of claim 2 wherein said first contiguous barrier layer is formed to a thickness X_2 on said trench sidewalls of said second trench.

Claim 5: The integrated circuit interconnect structure of claim 3 wherein the ratio X_1 to X_2 is greater than 3 to 2.

Claim 6: The integrated circuit of claim 1 further comprising a second contiguous barrier layer formed over said first contiguous barrier layer and beneath said copper.

Claim 7: A copper integrated circuit interconnect structure, comprising:

a low K dielectric layer with an upper surface formed over a semiconductor;

a plurality of trenches formed in said low K dielectric layer wherein said plurality of trenches has sidewalls;

a first contiguous barrier layer formed to a thickness X_1 over said upper surface of said low k dielectric layer and formed to a thickness X_2 over said sidewalls of said plurality of trenches wherein the ratio of X_1 to X_2 is greater than 3 to 2; and

copper formed over said first contiguous barrier.

Claim 8: The integrated circuit interconnect structure of claim 7 wherein said plurality of trenches are separated from each other by a distance of less than 160nm.

Claim 9: The integrated circuit interconnect structure of claim 7 further comprising a second contiguous barrier layer formed over said first contiguous barrier layer and beneath said copper.

Claim 10: The interconnect structure of claim 7 wherein the dielectric constant of the low K dielectric layer is less than or equal to approximately 3.7.

Claim 11: A method for forming a copper interconnect structure, comprising:

forming a low K dielectric layer with an upper surface over a semiconductor;

forming a plurality of trenches in said low K dielectric layer wherein said plurality of trenches has sidewalls;

forming a first contiguous barrier layer to a thickness X_1 over said upper surface of said low k dielectric layer and to a thickness X_2 over said sidewalls of said plurality of trenches wherein the ratio of X_1 to X_2 is greater than 3 to 2; and

forming copper over said first contiguous barrier.

Claim 12: The method of claim 11 wherein said plurality of trenches are separated from each other by a distance of less than 160nm.

Claim 13: The method of claim 12 further comprising forming a second contiguous barrier layer over said first contiguous barrier layer and beneath said copper.

Claim 14: The method of claim 13 wherein the dielectric constant of the low K dielectric layer is less than or equal to approximately 3.7.

Claim 15: A method for forming an integrated circuit copper interconnect structure, comprising:

forming a low K dielectric layer with a dielectric constant less than or equal to approximately 3.7 with an upper surface over a semiconductor;

forming a plurality of trenches separated by a distance of less than 160nm in said low K dielectric layer wherein said plurality of trenches has sidewalls;

forming a first contiguous barrier layer to a thickness X_1 over said upper surface of said low k dielectric layer and to a thickness X_2 over said sidewalls of said plurality of trenches wherein the ratio of X_1 to X_2 is greater than 3 to 2; and

forming copper over said first contiguous barrier.

Claim 16: The method of claim 15 further comprising forming a second contiguous barrier layer over said first contiguous barrier layer and beneath said copper.